

Fig.2c

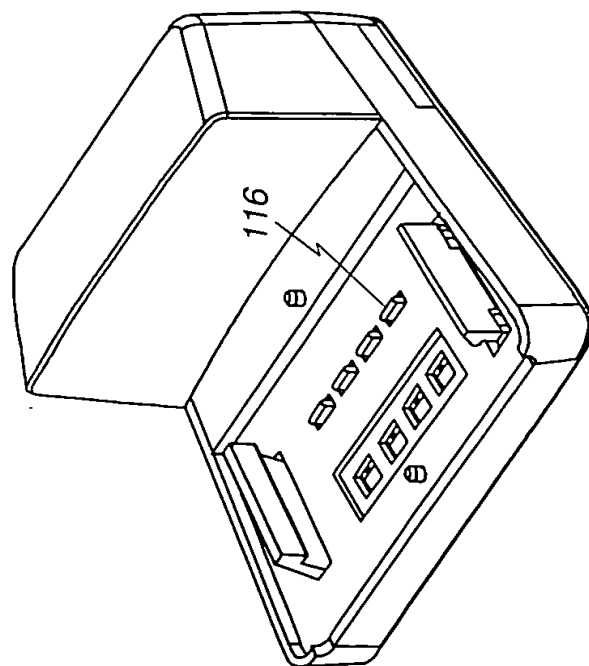
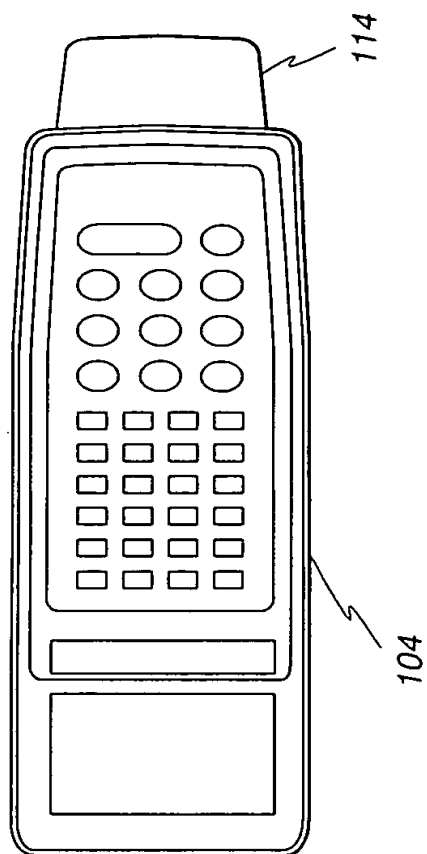


Fig.2a

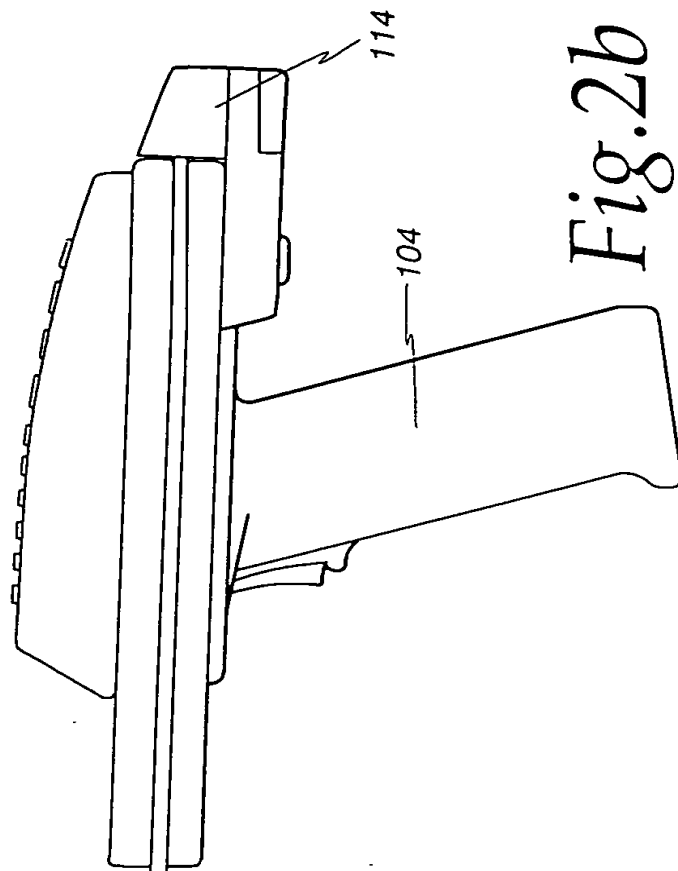


Fig.2b

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Fig.4

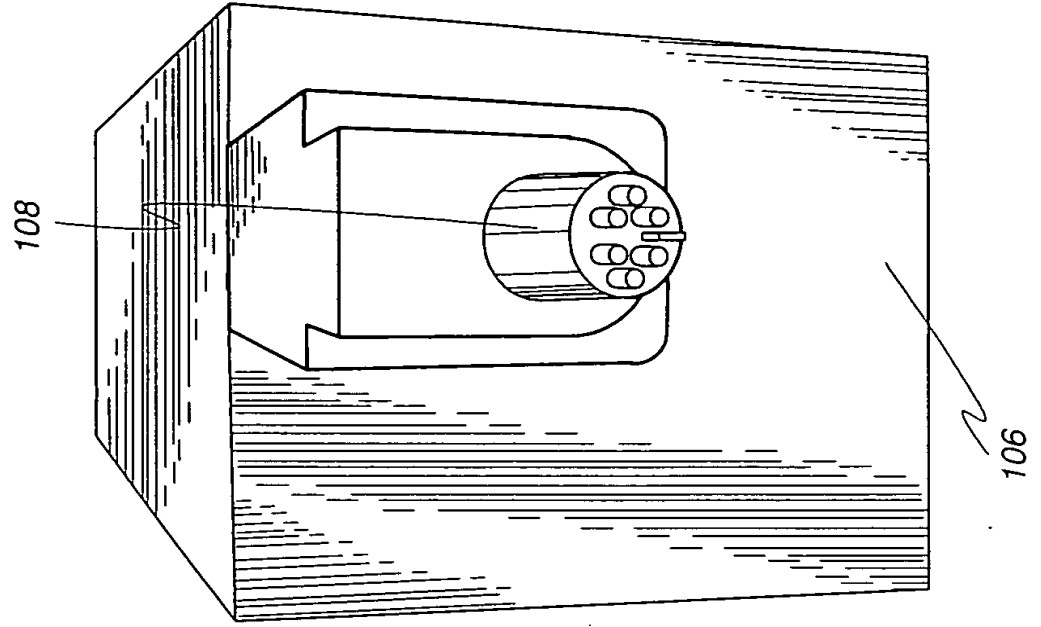


Fig.3

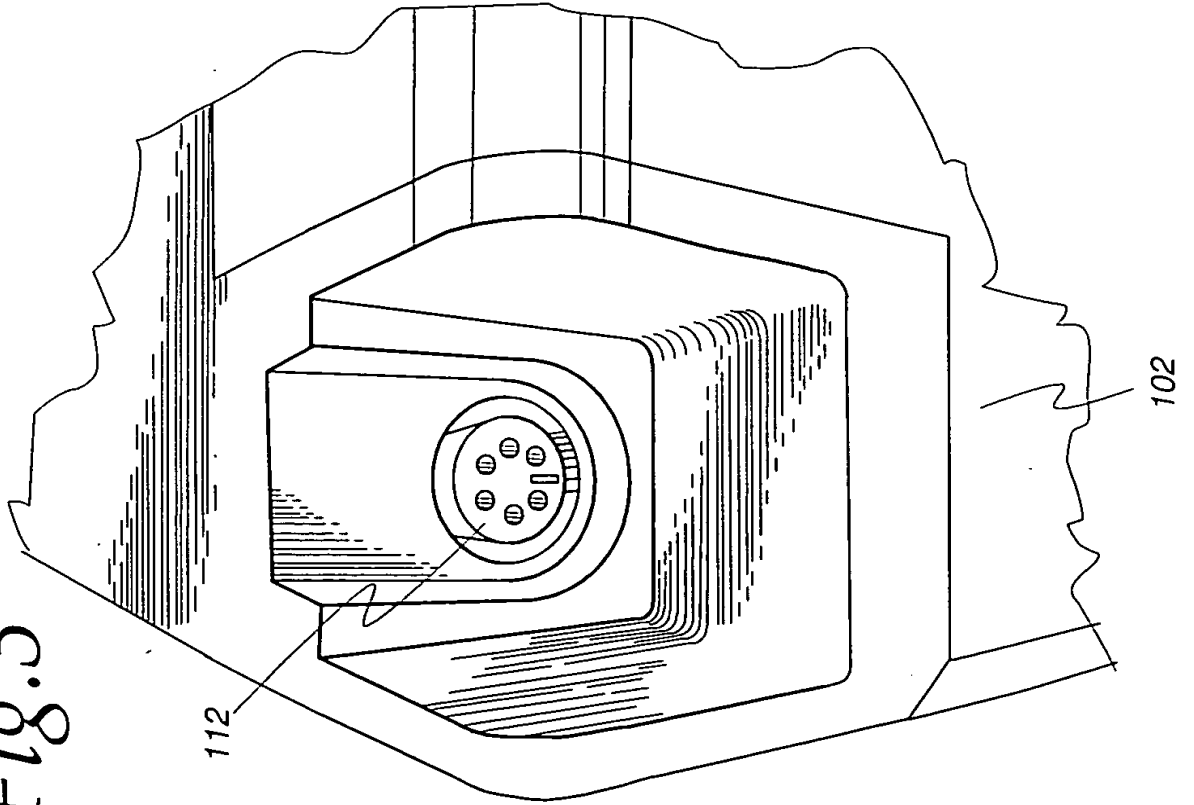
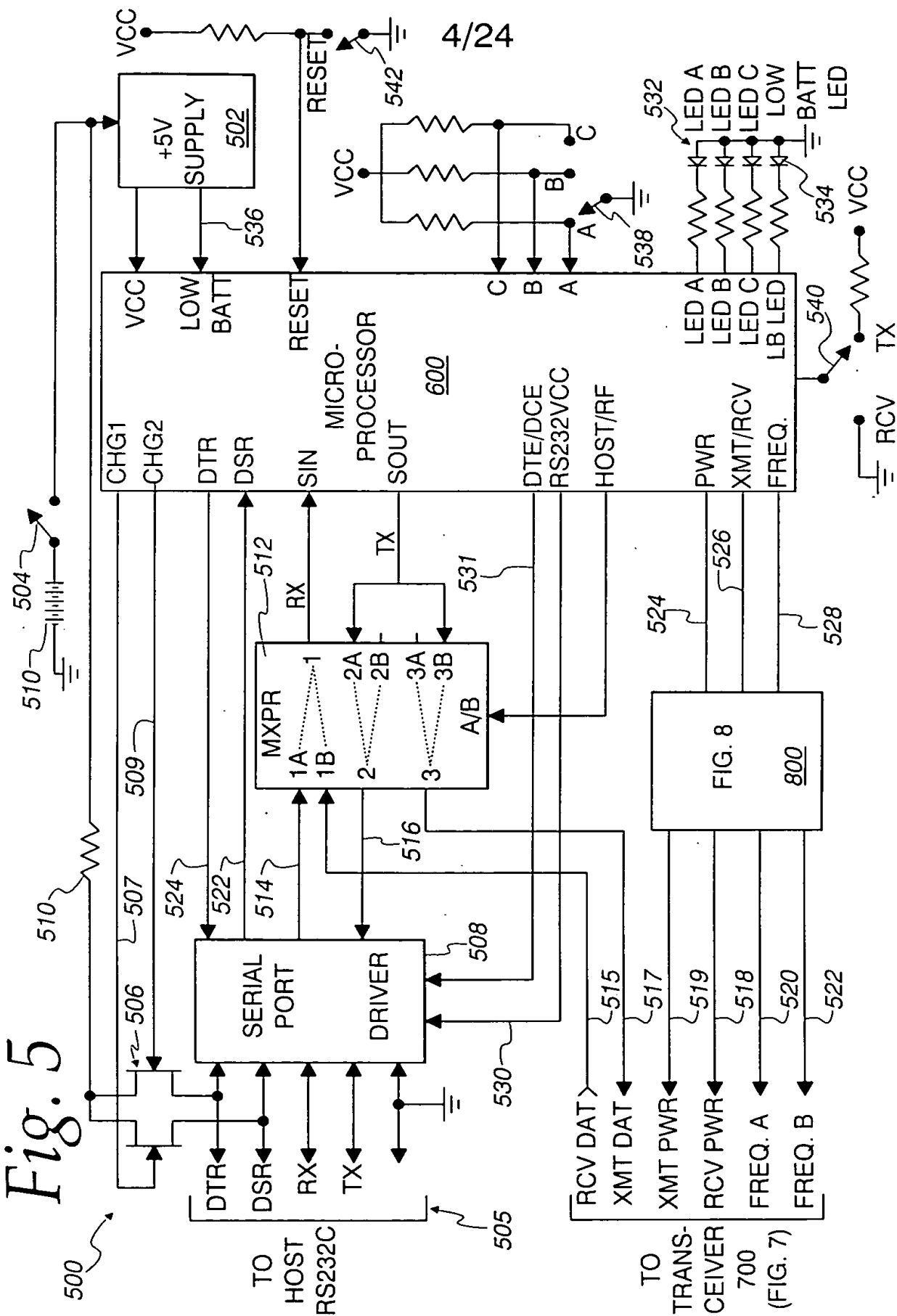


Fig. 5



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Fig. 6

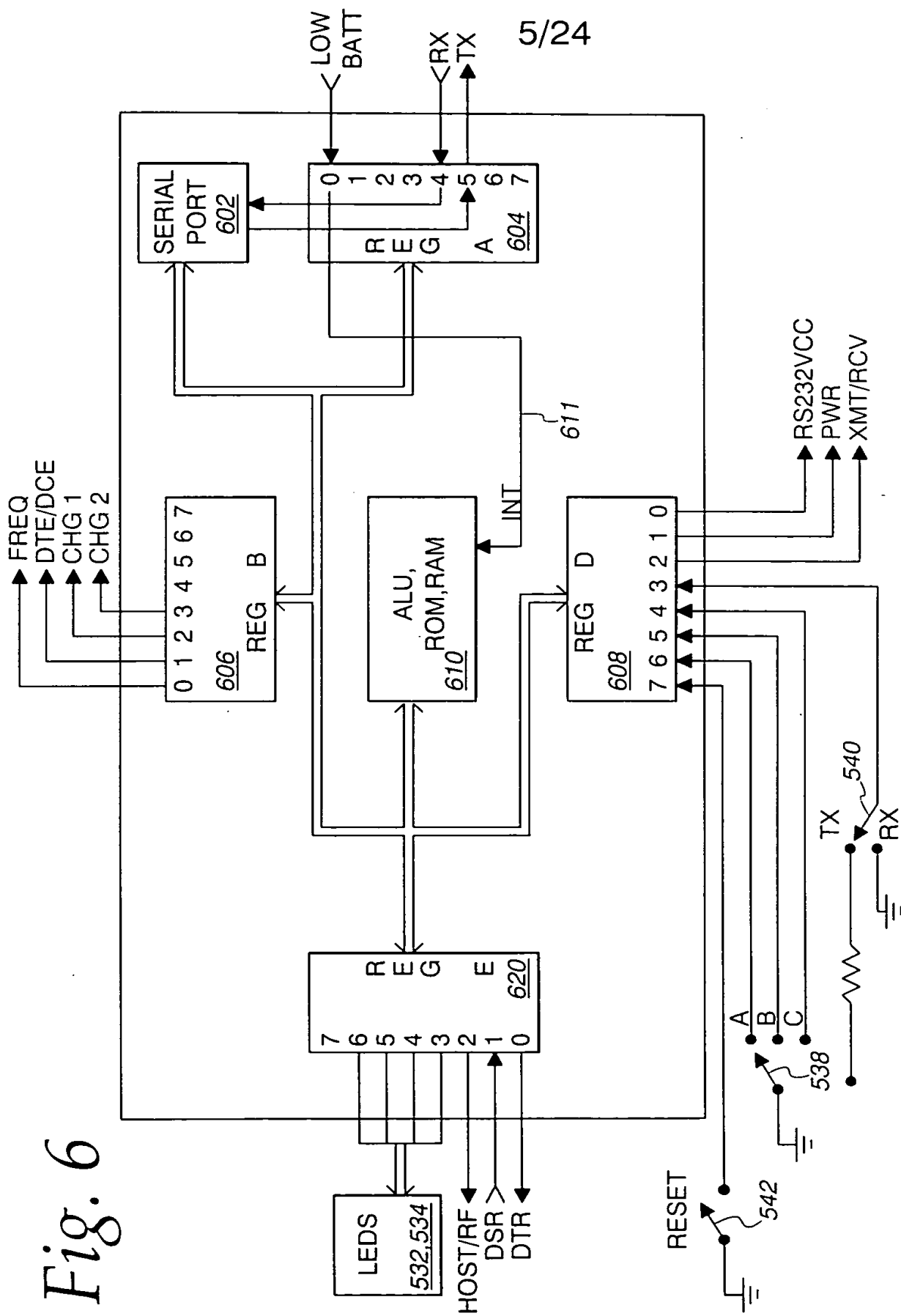
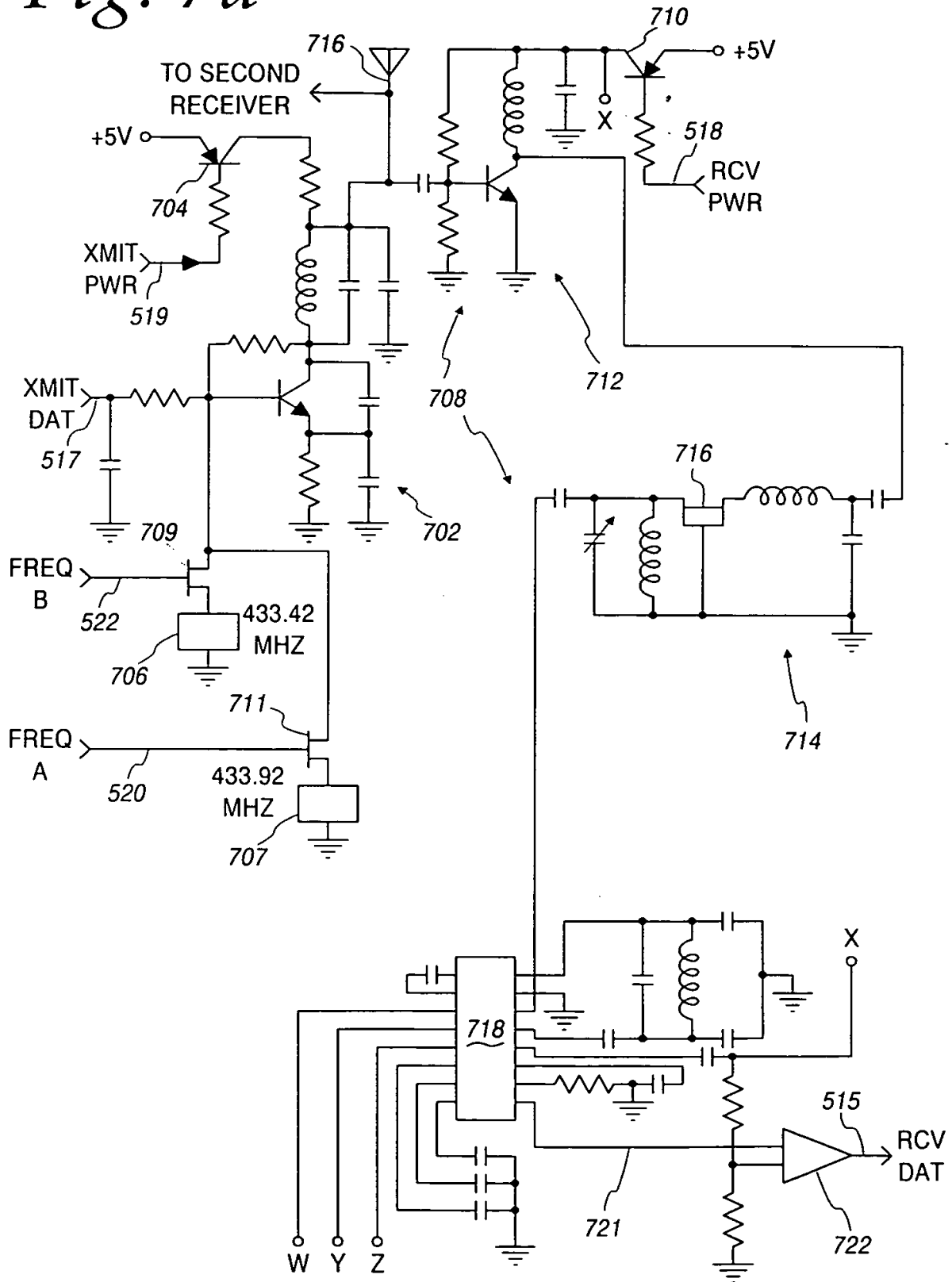


Fig. 7a

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Fig. 7b

The circuit diagram, labeled 719, shows a frequency divider circuit. It includes a PNP transistor 711. The base of the transistor is connected to a terminal labeled 'FREQ A' through a resistor 520. The emitter of the transistor is connected to a common ground line at the bottom of the circuit. The collector of the transistor is connected to a terminal 'X' through a resistor. A capacitor is connected between terminal 'X' and the common ground line. A resistor is connected between the collector of the transistor and a terminal 'Y'. A series combination of a capacitor and an inductor is connected between terminal 'Y' and the common ground line. The inductor is labeled '433.42 MHZ'. A terminal 'Z' is connected to the common ground line. The output of the circuit is taken from terminal 'Y'.

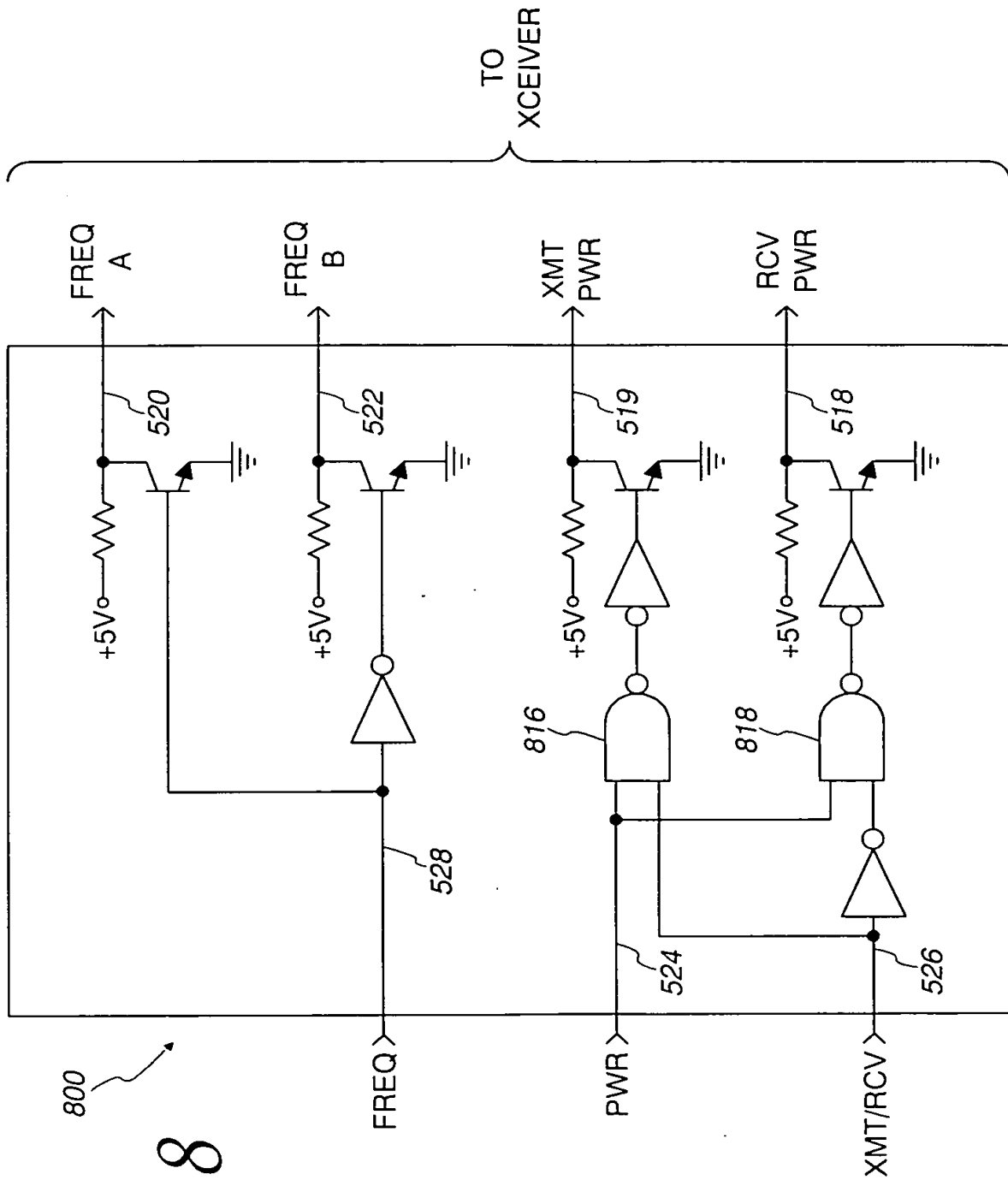
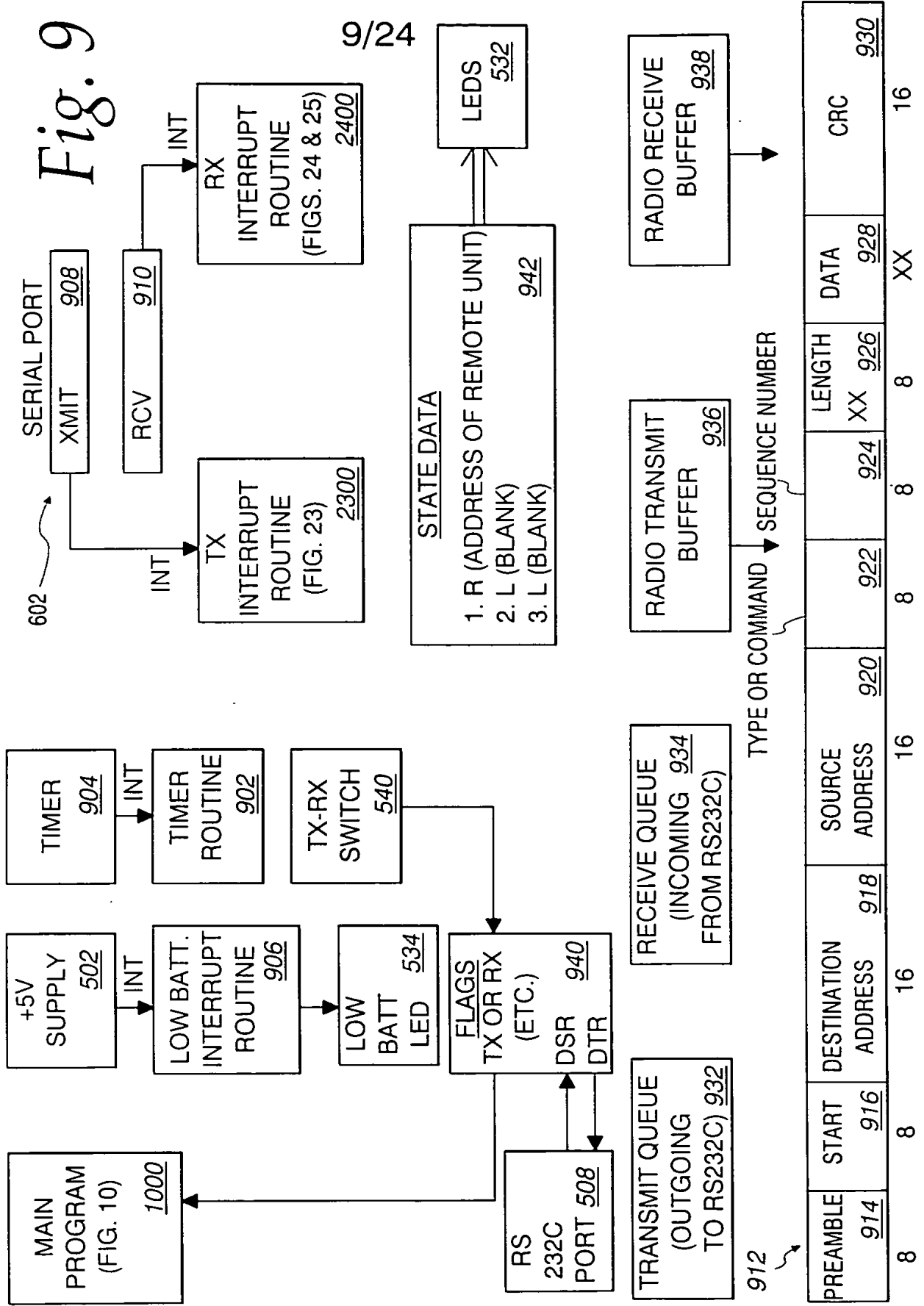


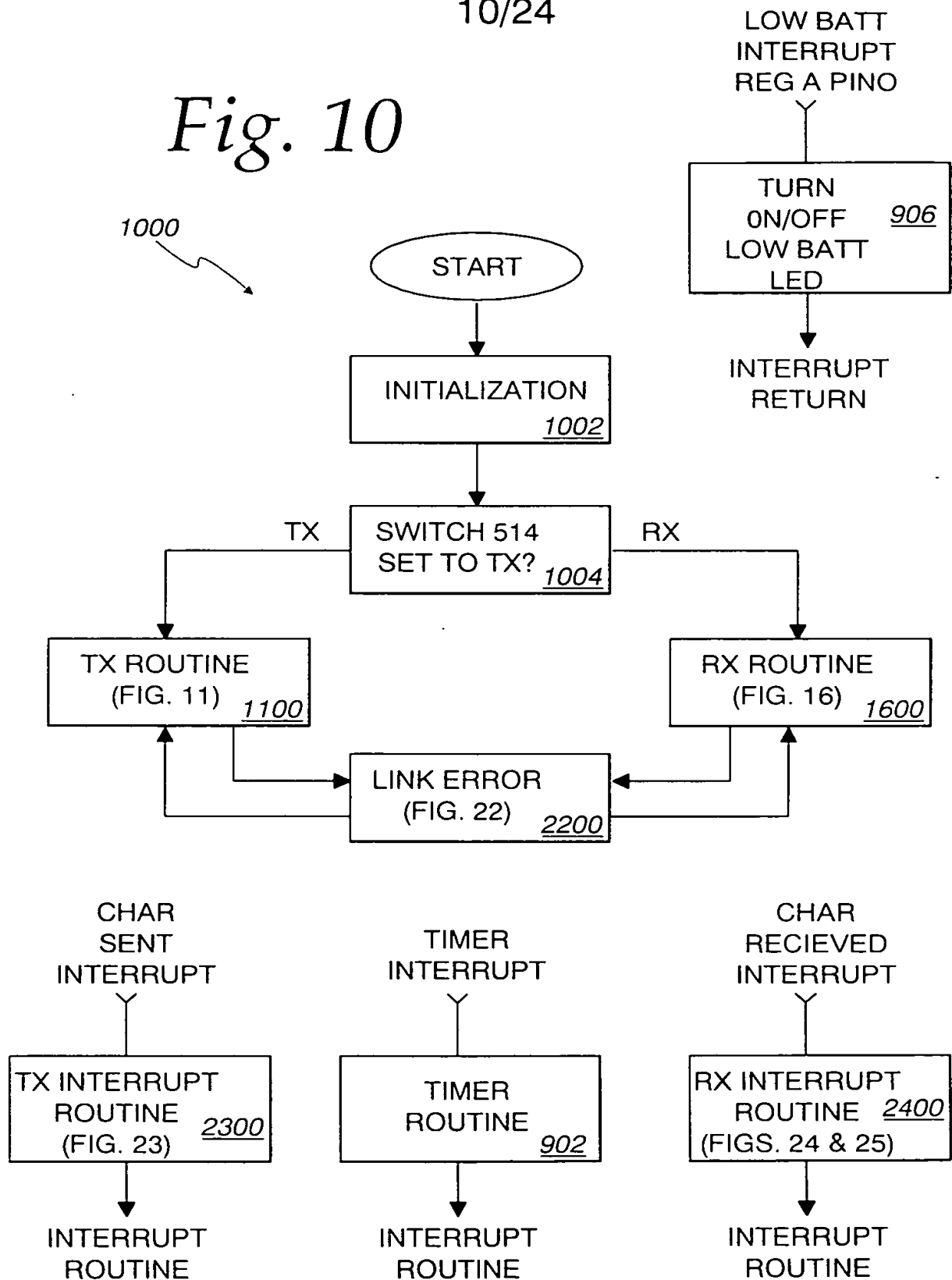
Fig. 8





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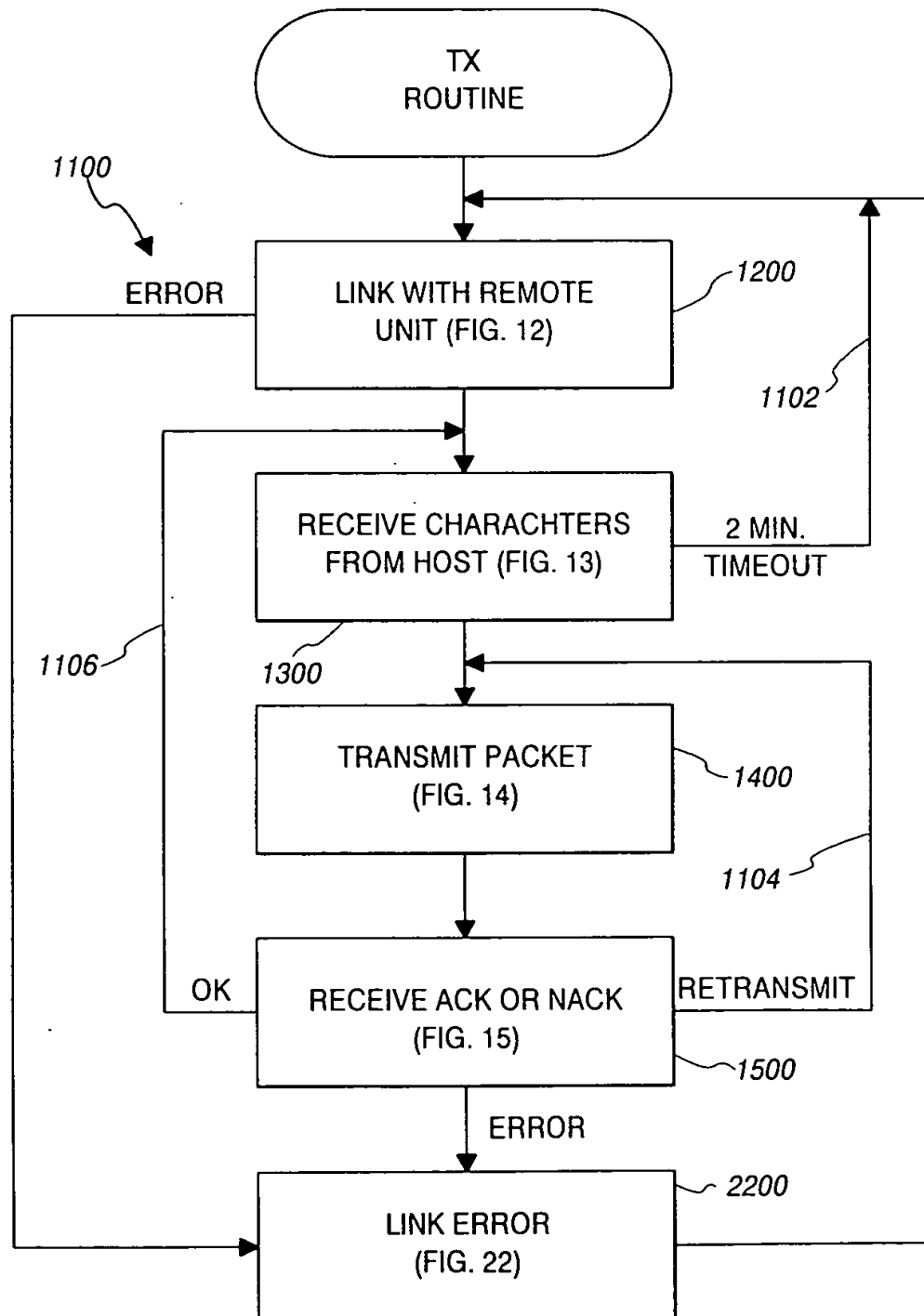
Fig. 10



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*Fig. 11*



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Fig. 12

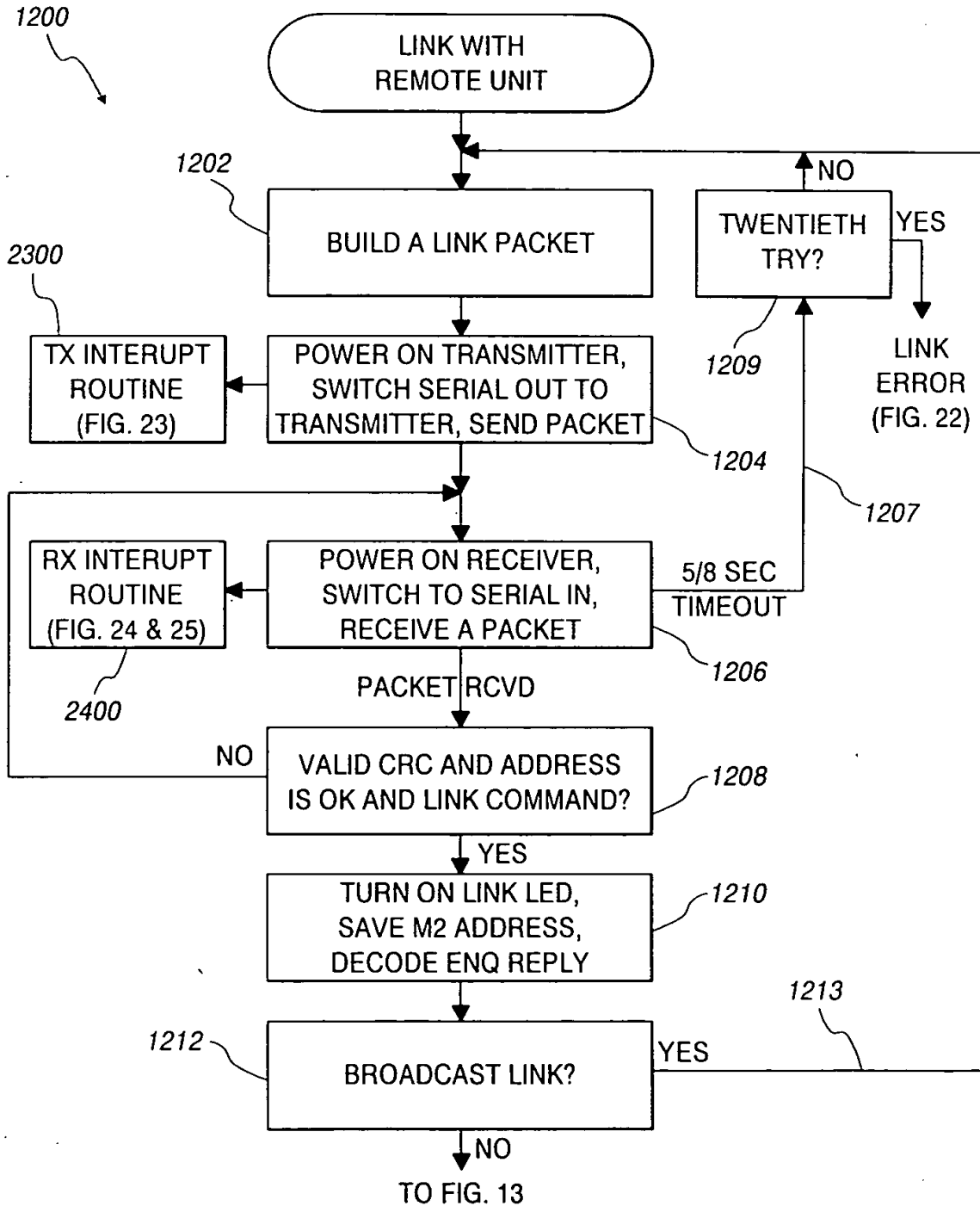
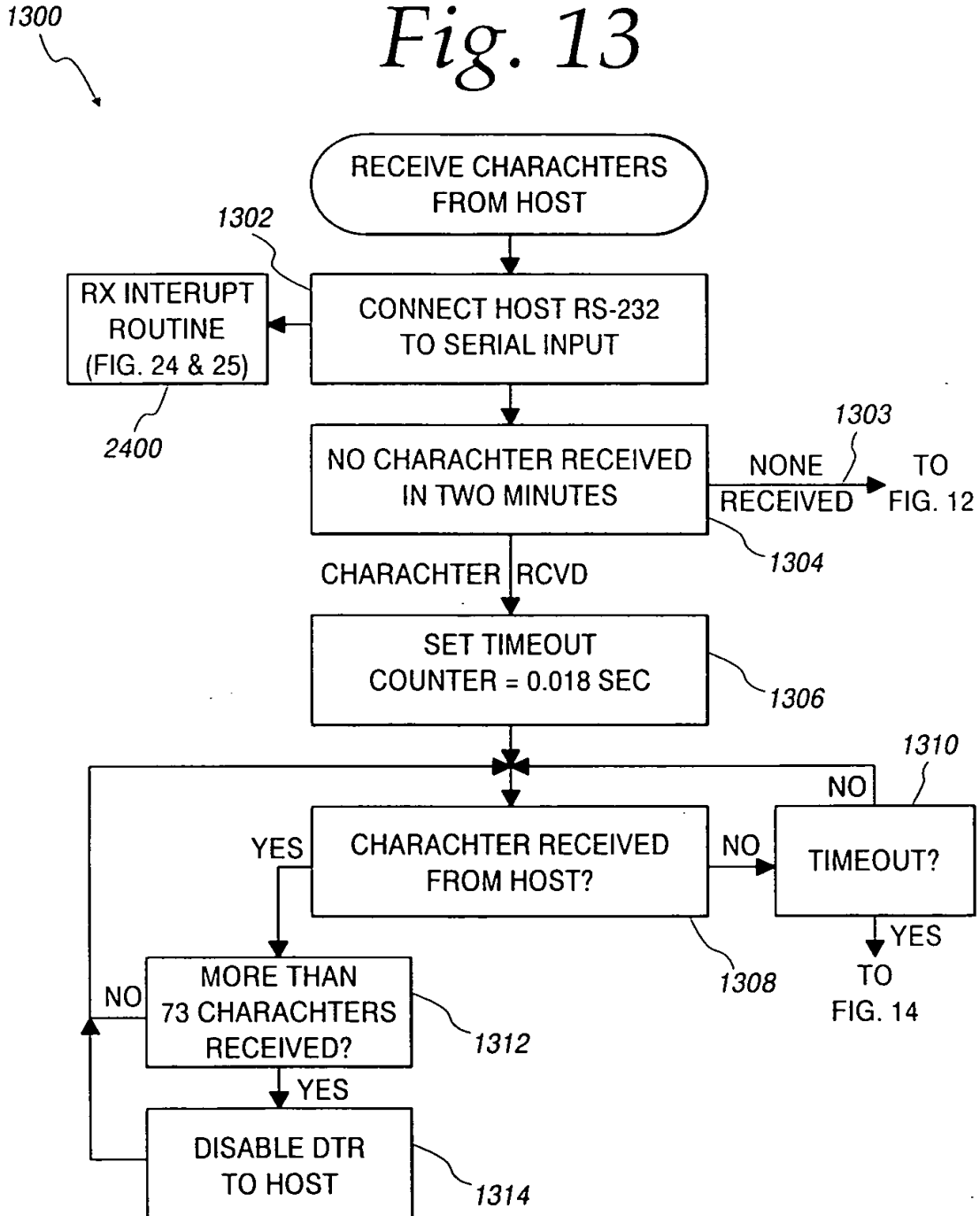
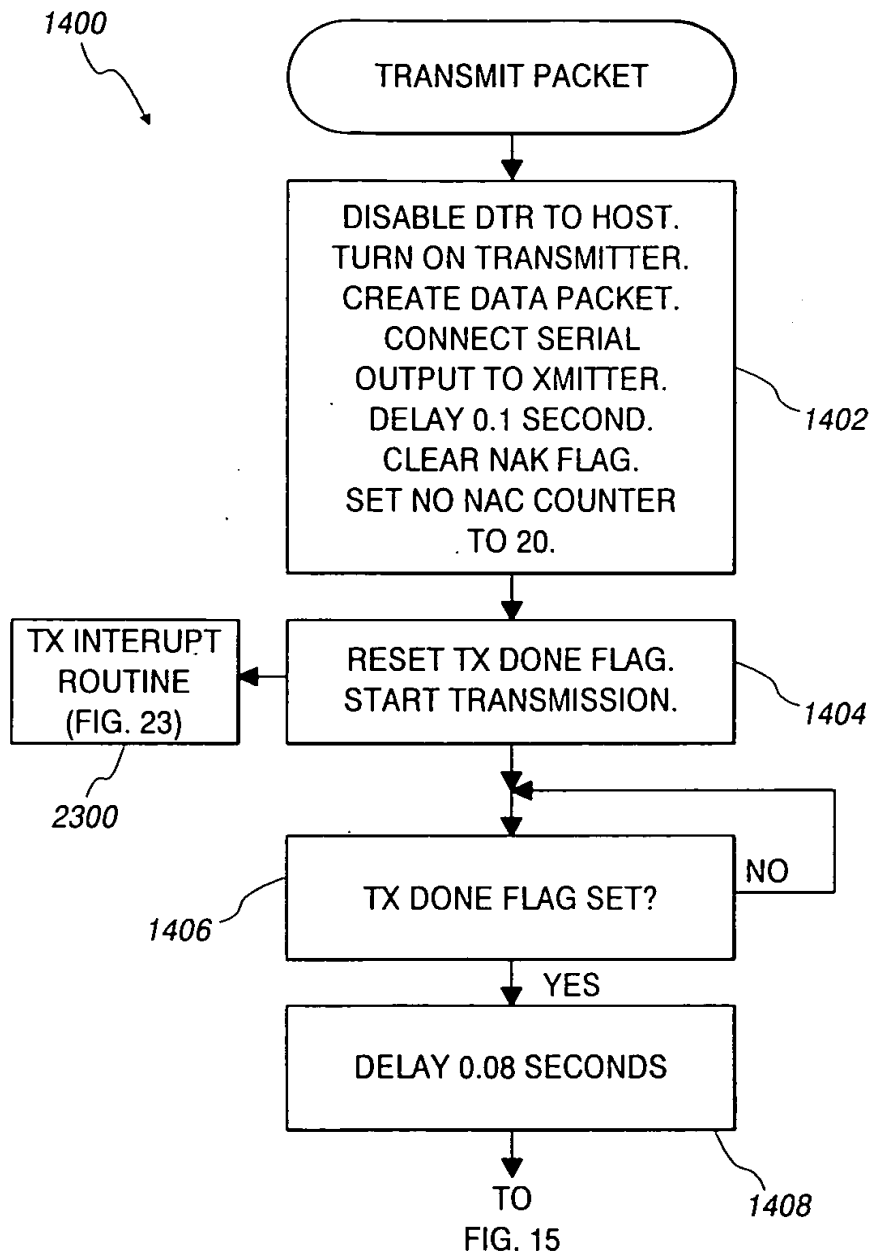
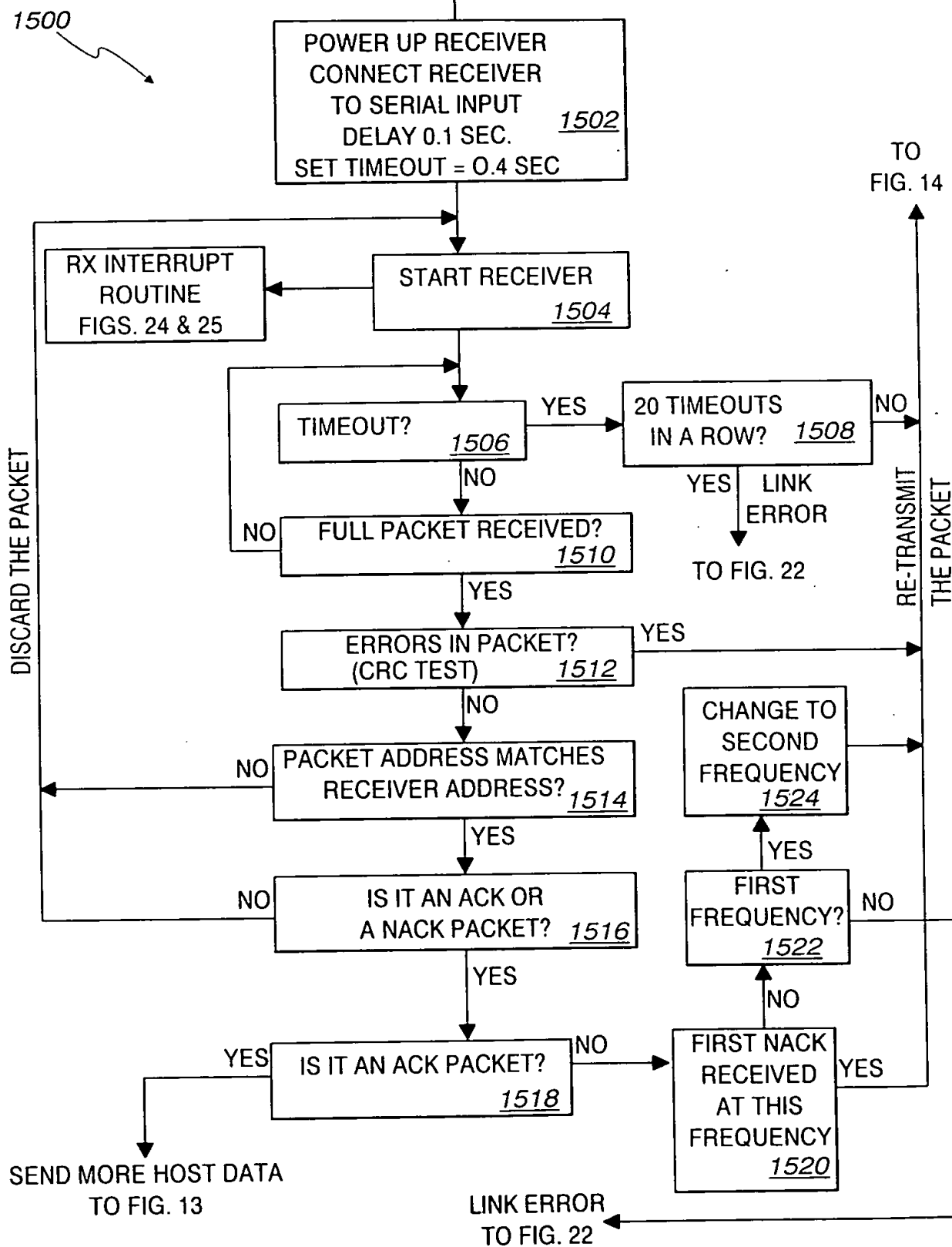
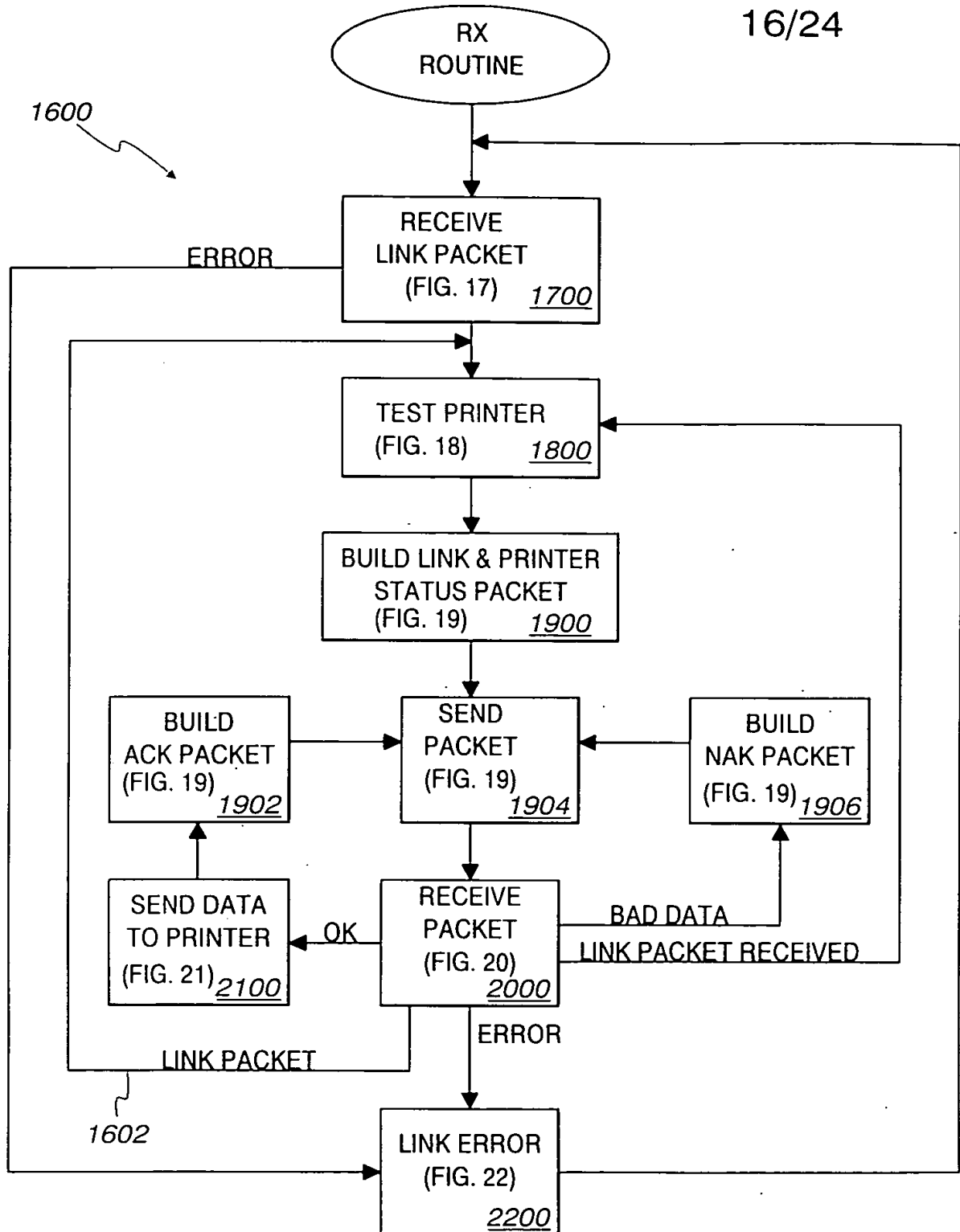


Fig. 13



*Fig. 14*

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*Fig. 16*



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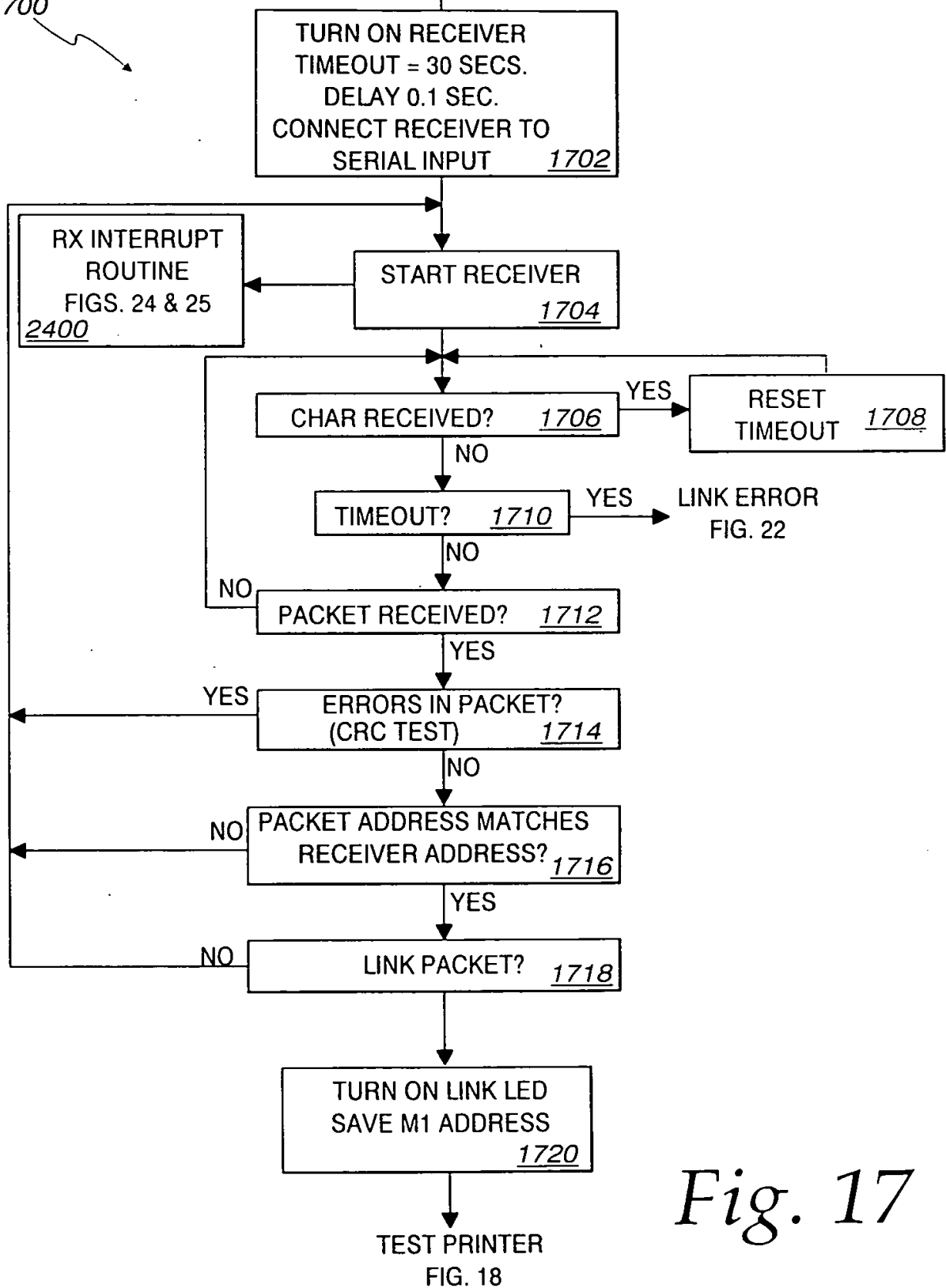
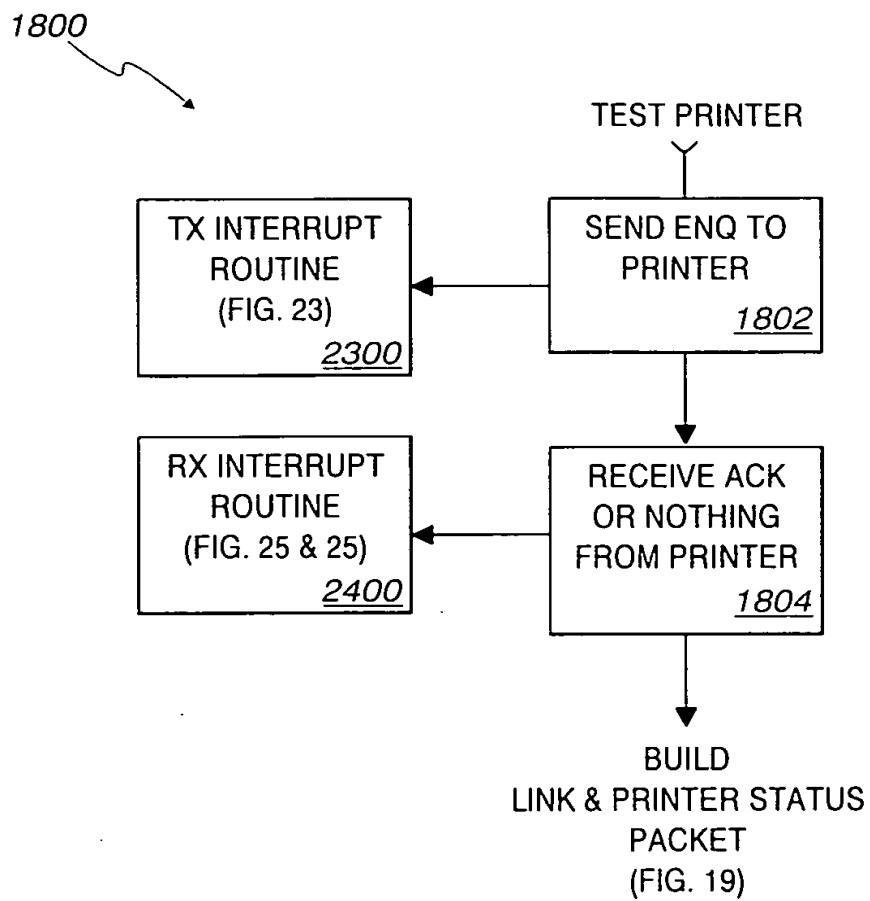


Fig. 17

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*Fig. 18*

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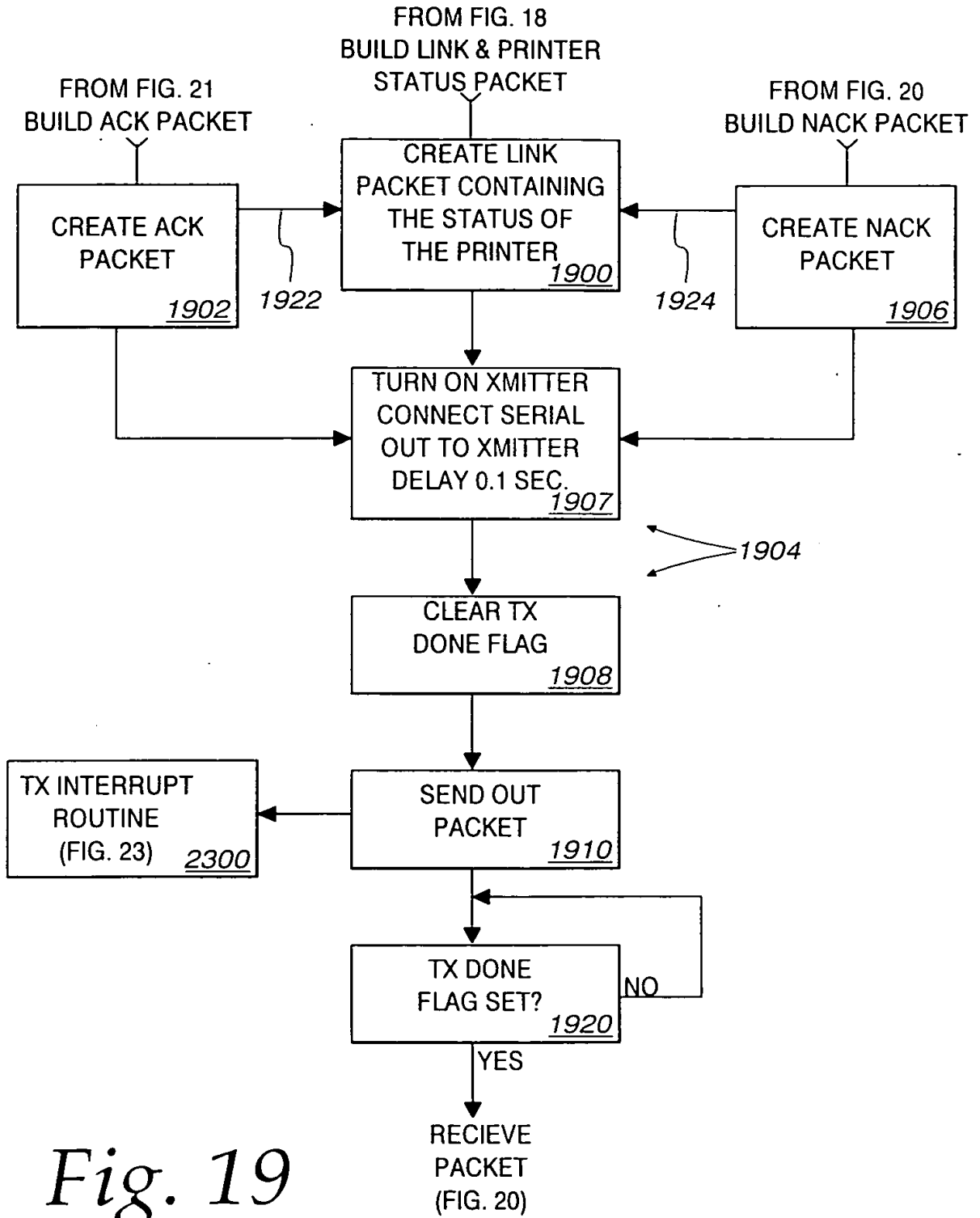
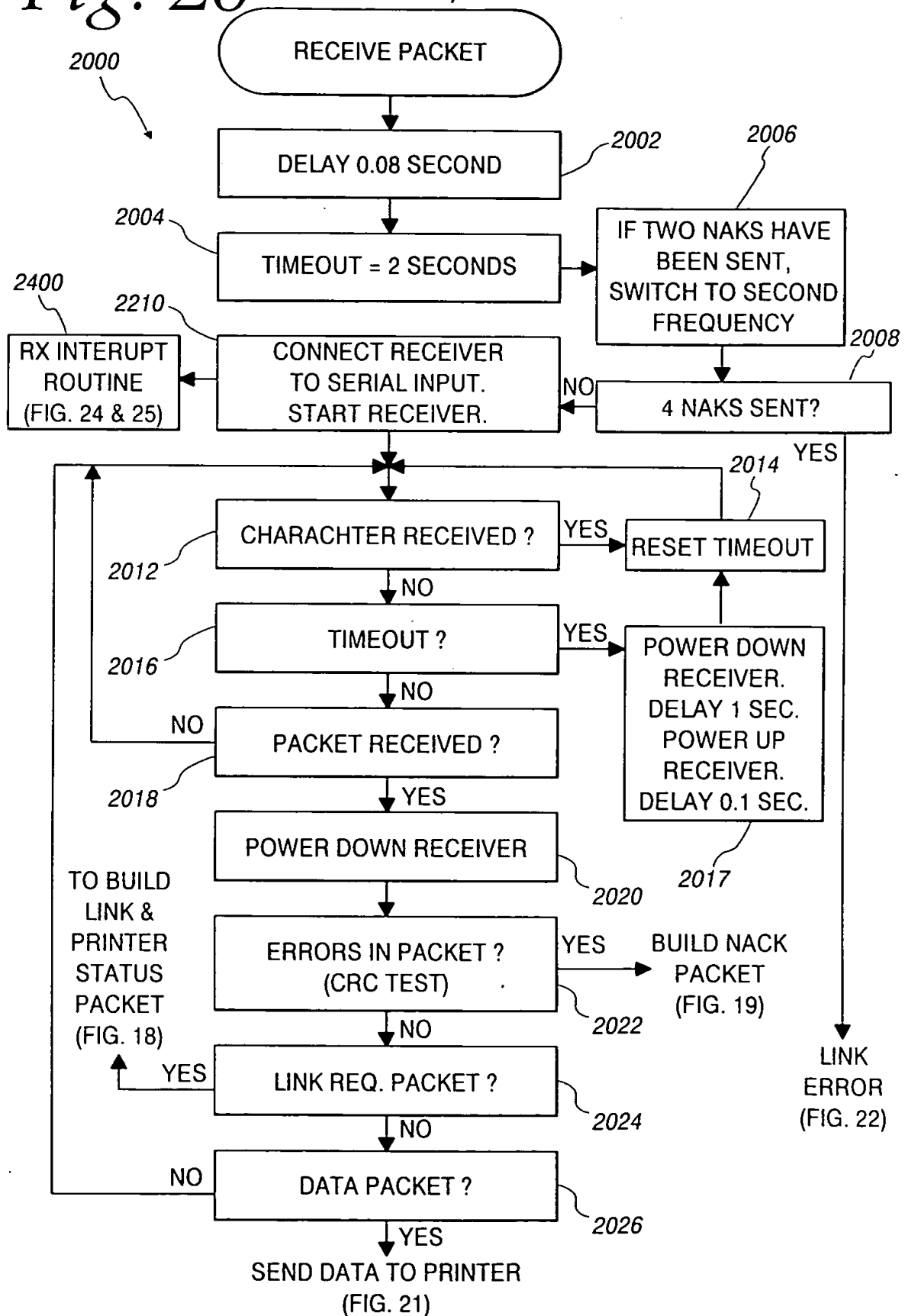


Fig. 19

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Fig. 20

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Fig. 21

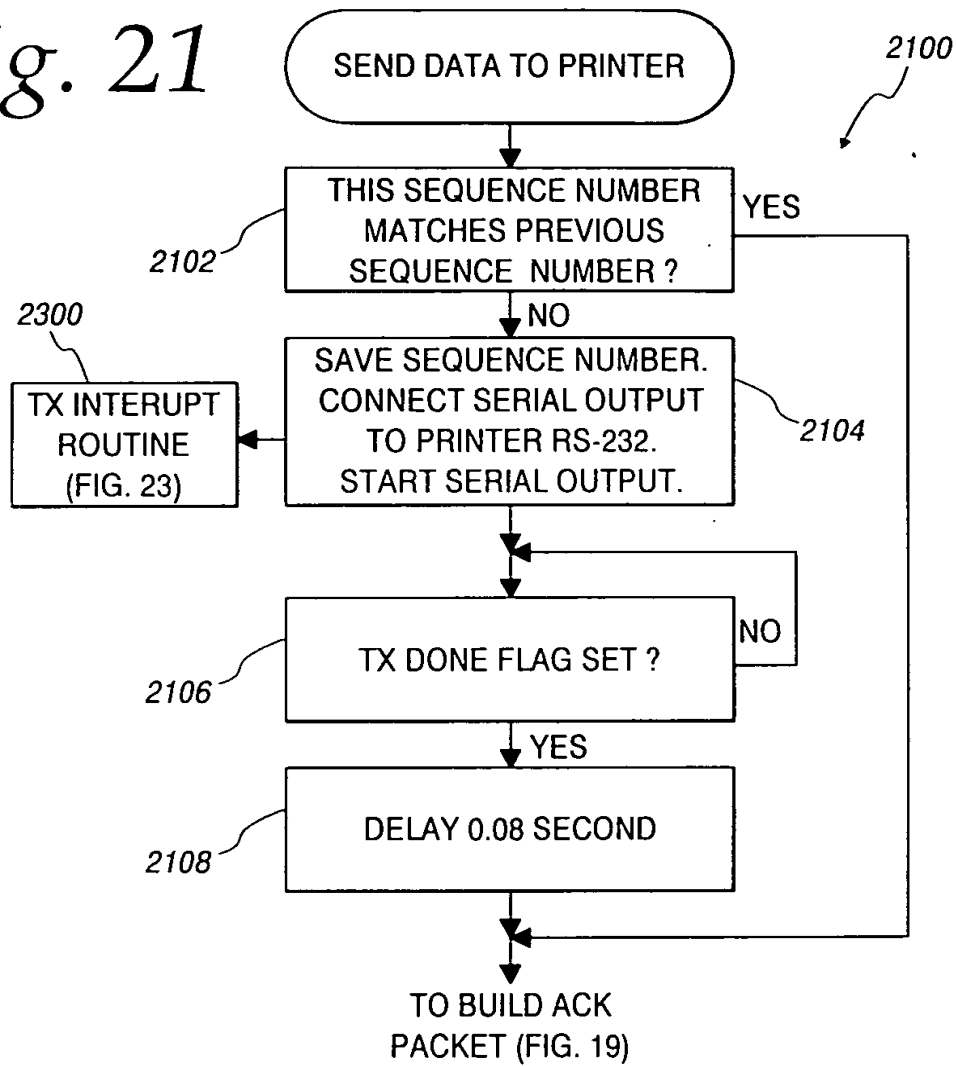
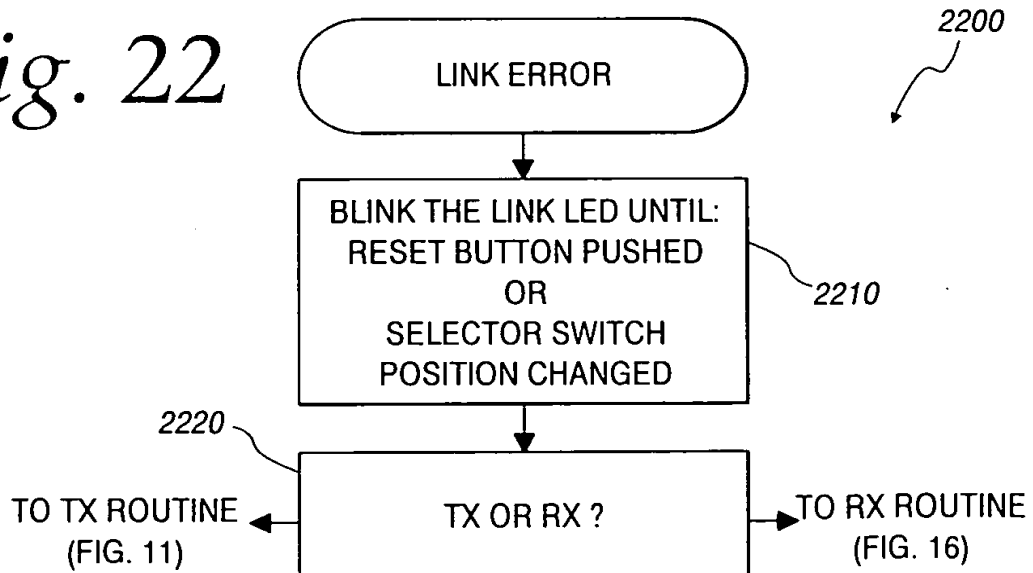


Fig. 22



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Fig. 23

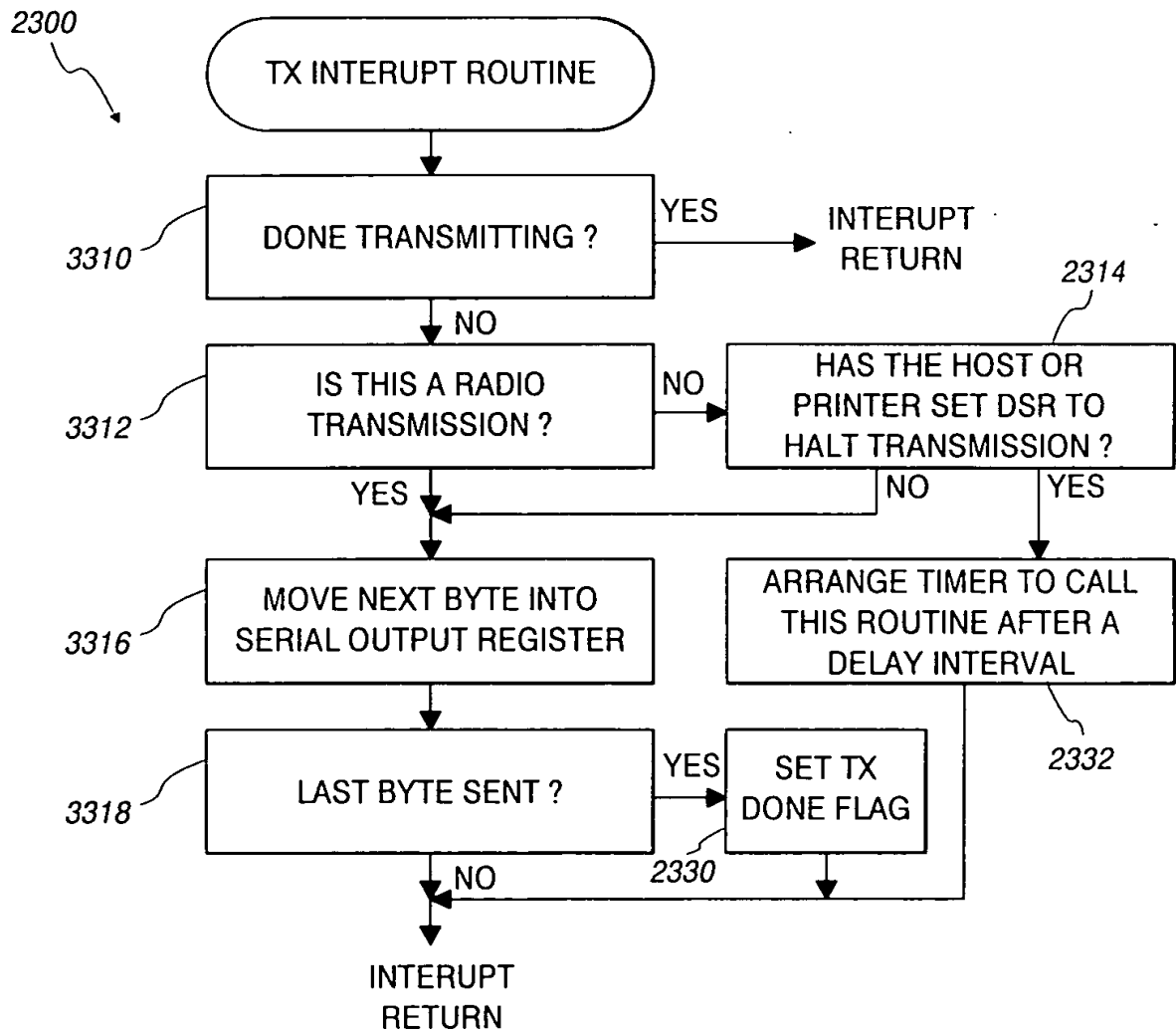
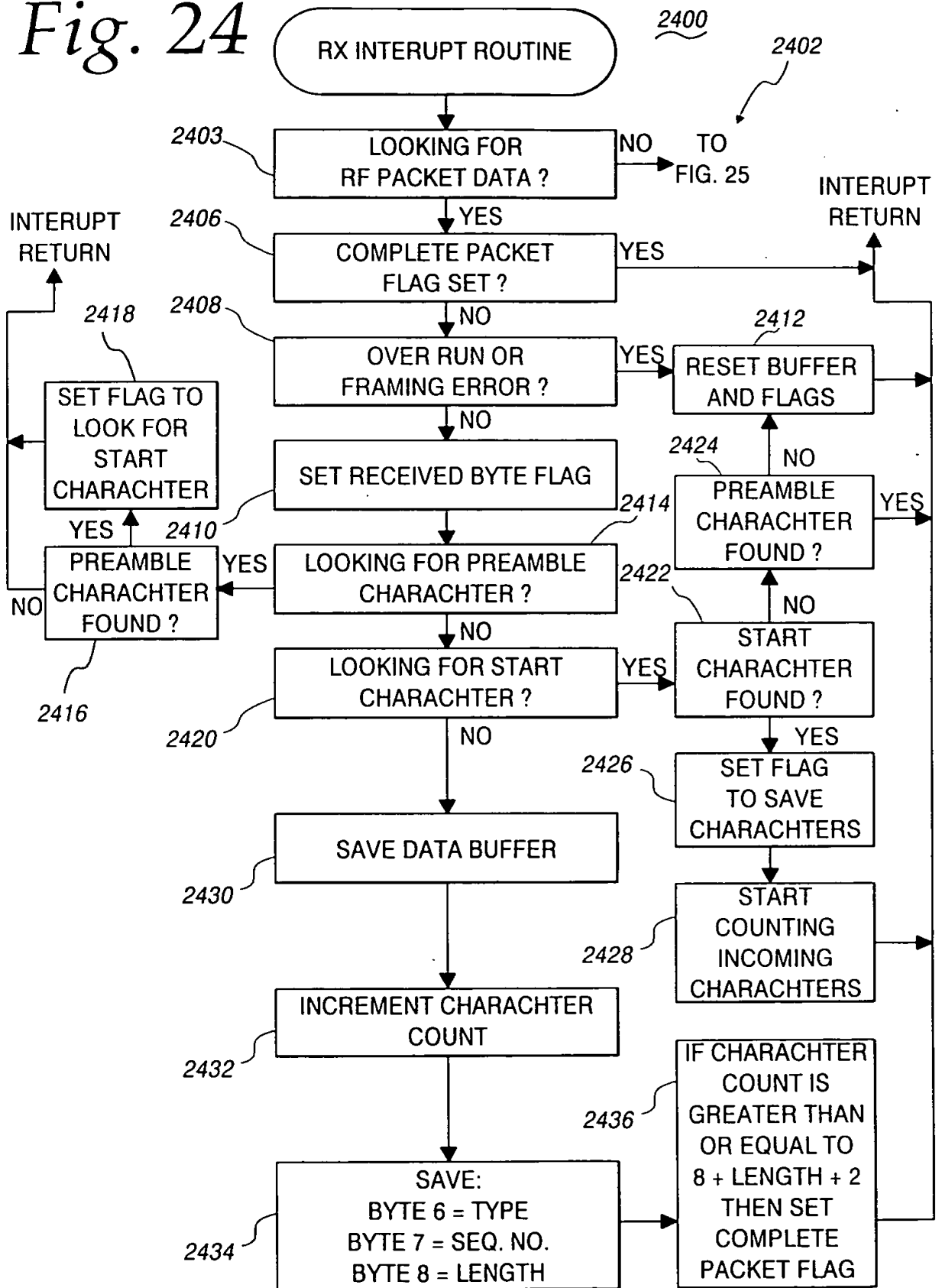
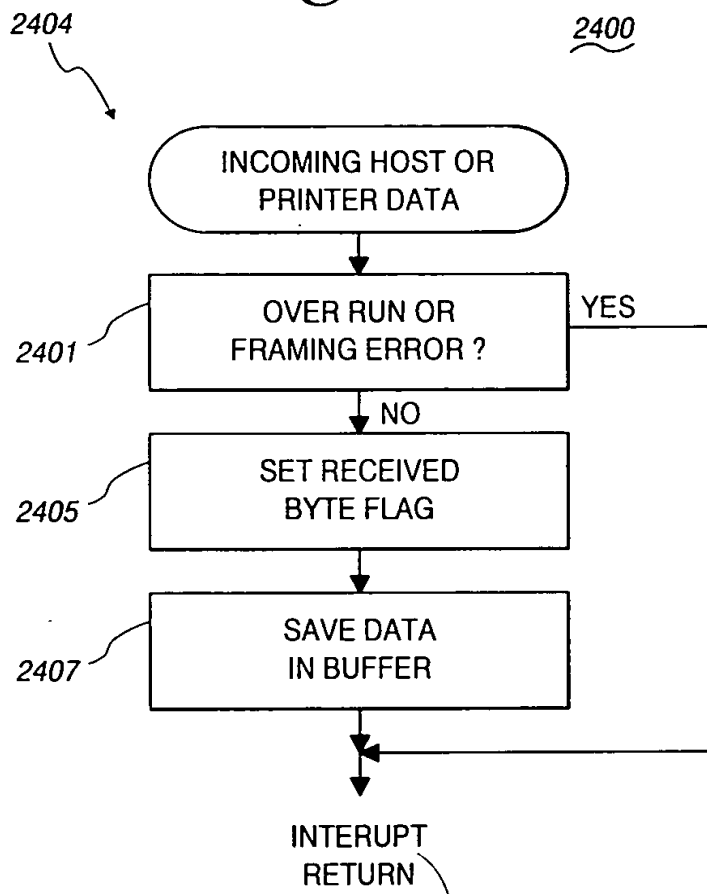


Fig. 24



*Fig. 25*

[illegible]